REMARKS

Claims 4-6, 8, 9, and 13-20 are pending in this application. Claims 1-3, 7, and 10-12 are cancelled and claims 16-20 are added herein. Claims 4-6, 13, and 14 have been amended herein. In view of these amendments and remarks, Applicant respectfully requests reconsideration of the claims.

The Examiner objected to the drawings for not showing every feature of the invention specified in the claims. Proposed replacement sheets for FIGs. 1 and 4 are provided herewith. FIGs. 1 and 4 have been corrected to show that the differential amplifier can be a comparator circuit 70a, and that an edge detecting circuit 70b may be included in the differential amplifier circuitry. FIG. 4 has further been corrected to show a multiplexing circuit 70c included in the differential amplifier circuitry. As discussed in more detail below, no new matter has been added as these features were clearly discussed and/or included in both the specification and claims of the original application. If these changes are acceptable to the Examiner, formal replacement sheets can be provided immediately.

Claims 1-15 were rejected under 35 U.S.C. 112, first paragraph as failing to comply with the enablement requirement in that the Examiner alleges that the description of the preferred embodiment in the specification is incomplete. Applicant respectfully disagrees and, as shown in the following paragraphs, a person skilled in the art would have no problem understanding and practicing the invention as originally presented. However, to expedite prosecution of the application, one or two very minor changes have been made to the drawings and specification to better present the invention. These changes along with the following discussion clearly show

that the description and drawings do comply with the 35 U.S.C. 112 enablement requirements and that a person with ordinary skill in the art can understand and practice the invention.

More specifically, the Examiner states that the differential amplifier 70 is not functioning as a differential amplifier because it has too many inputs and that the limitations that recite a comparator are misdescriptive. However, as the Examiner is probably well aware, a "comparator" is nothing more than a differential amplifier followed by a NAND gate and that the terms are often used interchangeably. See attached Exhibit A, where a comparator is considered to be a differential amplifier. Also, see Exhibits B, C, and D. Further, commercially available "operational amplifier" (OP amps) are typically multifunctional and can operate as amplifiers, buffers, comparators, differential amplifiers, etc., etc., etc. See attached Exhibit E, a PREM® (Fairchild Semiconductor) Electronic products Data Sheet that provides information about the evolution of monolithic op amps (specifically see the highlighted portions on page 3 of Exhibit E).

Also as indicated on page 2 of Exhibit F, multi-input comparators have been commercially available for a long time and are still available. As indicated by Exhibit F, the multiple input comparator may include an internal multiplexer to handle the various inputs. In any event, it is seen that a person skilled in the art would understand and could practice the invention based on the disclosure in the application.

Claims 1-15 were also rejected under 35 U.S.C. 112, second paragraph as being indefinite because of use of the term "differential amplifier". However, as was discussed above, a comparator is a differential amplifier followed by a NAND gate, and a person skilled in the art would fully understand the application and how to practice the invention.

The Examiner objected to the use of the term "edge detector" in claim 3, and required applicant to point out how that limitation reads on the circuit arrangement of the drawings. The function and operation of an edge detector is well known and understood by anyone skilled in the art. Further, the specification along with FIGs. 2 and 3 discuss how the edge detectors determine whether a pulse edge is rising or falling. In addition, both FIGs. 1 and 4 now illustrate that the edge detector may be part of the "differential amplifier" circuitry.

In addition, the last paragraph of page 8 and the second paragraph of page 9 of the Applicant's specification support the use of the terms "comparator" and "edge detector". For example, the second paragraph of page 9 describes a second variation of the first embodiment as outputting a binary signal dependent on the results of a comparison to a specific threshold [voltage] and whether the detected edge of the pulse is moving positive or negative. This clearly indicated that the differential amplifier has the functionality of detecting the edge of a pulse and comparing the signal to a threshold.

With respect to the embodiment of FIG. 4, the Examiner argues that it is not shown how a differential amplifier having a large number of inputs can be operated. However, it is clear from the description on page 10, second paragraph to page 11, first paragraph that the functionality of the embodiment is such that a single differential amplifier is provided, which operates to select one desired input form a plurality of a first inputs and another desired input from a plurality of second inputs and that a difference output is generated from the signals received on the two inputs. Further, as discussed above, multi-input differential amplifiers are commercial and are readily available. Thus, the knowledge of a person of ordinary skill in the art in combination with the description on page 10, last paragraph to page 11, first paragraph clearly provides sufficient information for a person skilled in the art to implement the device as discussed by

switching a multiplexer between the respective inputs of the differential amplifier and the outputs of the delay elements.

With respect to the Examiner's objection on page 3 that the term comparator is misdescriptive, it is clear from page 8, last paragraph to page 9, second paragraph that the comparator simply determines whether a signal exceeds a specific threshold. This is precisely what comparators do. Therefore, it is not seen how the term comparator can be a misdescription.

Finally, with respect to the rejection of claims 12 and 15, the Examiner is referred to page 9, lines 14 to 10, which describes the detector of an edge of the partially delayed signal and to the last paragraph of page 9, which describes that the "bit" is decoded by means of a differential signal.

Claims 1-15 were further rejected under 35 U.S.C. 102(b) as being anticipated by Morishima. Applicant respectfully disagrees. More specifically, the Morishima reference only describes a differential amplifier circuit receiving a first signal, which is delayed for a first period of time and then is further delayed by a second period of time. An output signal is generated by these two delayed versions of the signal. However, the Morishima reference does not even mention, much less teach, that the input signals are bipolar signals having a positive part and a negative part of the same duration, as specified in each independent claim.

With regard to claim 4, it is further noted that nothing in the Morishima reference teaches or suggests that the amplifier is implemented to compare the difference signal to a first and to a second threshold and to also determine whether the signal has a rising or a falling edge. Further, Morishima certainly does not teach that an output binary signal is being provided on the basis of this information.

The Examiner's conclusions regarding the rejection of claim 8 under 35 U.S.C. 102(b) is also incorrect. Morishima does not teach a device for transmitting a "bit". More specifically, the driving circuit of Morishima does not generate a bipolar pulse with a positive part and a negative part of the same duration for providing transmission of a "bit".

Further, it is noted that nothing in the Morishima reference mentions, much less teaches, providing a plurality of delay elements and selecting a first and second input from a plurality of first inputs and a plurality of second inputs depending on the duration of the positive portion and the negative portion of the input bi-polar pulses.

In view of the above, Applicant respectfully submits that the application is in condition for allowance and requests that the Examiner pass the case to issuance. If the Examiner should have any questions, Applicant requests that the Examiner contact Applicant's attorney at 972-732-1001 so that such issues may be resolved as expeditiously as possible. In the event that the enclosed fees are insufficient, please charge any additional fees required to keep this application pending, or credit any overpayment, to Deposit Account No. 50-1065.

Respectfully submitted,

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Date

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